

2. A nonvolatile semiconductor memory device according to claim 1, wherein the semiconductor memory device is a NOR-type memory device.

3. A nonvolatile semiconductor memory device according to claim 1, further comprising a write driver and a sense amplifier.

21 4. A nonvolatile semiconductor memory device according to claim 3, wherein the write driver and sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation.

5. A sector structure of a nonvolatile semiconductor memory, said sector structure comprising:

a plurality of memory cell transistors arranged in a cell array block; and

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Cmpd. a plurality of decoder transistors arranged in a column decoder block, wherein said memory cell transistors and decoder transistors are arranged on a common bulk region.

6. A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein an erase operation is configured to erase all of the transistors in the sector simultaneously.

7. A sector structure of a nonvolatile semiconductor memory according to claim 5, said sector structure further comprising:

a plurality of word lines arranged in the cell array block, each word line being connected to a plurality of cell gates;

a plurality of bit lines arranged in the cell array block, each bit line being connected to a plurality of memory cell drains;

a plurality of common data lines connected to the bit lines;

a plurality of write drivers, each connected to a respective one of the common data lines; and

a plurality of sense amplifiers, each connected to a respective one of the common data lines.

8. A sector structure of a nonvolatile semiconductor memory according to claim 7, wherein each write driver and sense amplifier is configured to be placed in a state of high impedance during an erase operation.

9. A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein said sector structure is configured to provide 64 Kbytes of memory.

10. (Amended) A nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising:

a cell array block comprising a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of a plurality of word lines, each drain being connected to a corresponding bit line out of a plurality of bit lines;

a source line driver commonly connected to a source of each of the plurality of memory cell transistors and configured to apply a source voltage;

a column decoder block comprising a plurality of column decoder transistors, each column decoder transistor connected between one of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines; and

a common bulk region arranged in each sector and formed immediately adjacent to a substrate region, wherein the plurality of memory cell transistors and the plurality of column decoder transistors in each sector share the common bulk region; and

a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of that sector.

11. A nonvolatile semiconductor memory device according to claim 10, wherein the memory device is a NOR-type flash EEPROM.

12. A nonvolatile semiconductor memory device according to claim 10, wherein the bulk region is a pocket P-well.

13. A nonvolatile semiconductor memory device according to claim 10, further comprising a plurality of write drivers and sense amplifiers, wherein each data line is connected to a corresponding one of the write drivers and a corresponding one of the sense amplifiers.

14. A nonvolatile semiconductor memory device according to claim 13, wherein the write drivers and sense amplifiers are each configured to be placed in a state of high impedance during an erase operation.

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15. (Amended) A nonvolatile semiconductor memory device comprising:
a substrate;
a plurality of sector units, each sector unit comprising a common bulk region, the bulk region being formed on the substrate and connected to a bulk driver, and wherein each sector unit is configured to be electrically erasable in response to an erase signal; and
a plurality of memory cell transistors and transistors of a column decoder arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage.

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16. A nonvolatile semiconductor memory device according to claim 15, wherein each sector unit further comprises a bulk driver configured to supply a bulk voltage to the common bulk region.

17. A nonvolatile semiconductor memory device according to claim 15, wherein said plurality of memory cell transistors are arranged in a cell array block, wherein said plurality of column decoder transistors are arranged in a column decoder block, and wherein said cell array block and said column decoder block are both arranged on the common bulk region.

18. (Amended) A method of forming a bulk region of a nonvolatile semiconductor device, said method comprising:
forming a bulk region for memory cell transistors provided in a cell array block of the nonvolatile semiconductor memory device, wherein the cell array block is arranged in an (M x N) array with M and N both at least equal to two; and
forming a bulk region for decoder transistors of a column decoder in the bulk region for the memory cell transistors of the cell array block, wherein the column decoder is arranged in a (P x N) array with P at least equal to one.

19. A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, further comprising configuring the bulk regions for the memory cell transistors and decoder transistors to receive a common bulk signal during an erase operation.

20. A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, wherein said memory cell transistors and said decoder transistors are configured to be simultaneously erased with each other during an erase operation.

26. (New) The device of claim 1, wherein the cell array block and the column decoder block of each sector share a plurality of word lines and a plurality of bit lines.

27. (New) The device of claim 17, wherein the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one.